IN THE CLAIMS:

1. (original) A method of forming a trench memory device in a semiconductor substrate comprising the steps of:

etching a trench having trench axes parallel to <100> directions of said substrate, said trench having a square cross section in a lower portion and an octagonal cross section in an upper portion;

forming a liner layer of liner material on interior walls of said trench in said upper portion, whereby said liner layer has a first thickness on {100} surfaces of said interior walls;

etching said liner layer selective to the substrate, whereby said liner layer remains on said {100} surfaces and corners of said trench are exposed;

etching said interior walls selective to said liner layer, whereby said octagonal cross section is converted to a rectangular cross section having a trench wall width between trench corners.

2. (original) A method according to claim 1, in which said substrate is silicon and said liner material is selected from the group comprising $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$, further comprising a step of:

stripping said liner material from said interior walls after said step of etching said interior walls selective to said liner material.

3. (original) A method according to claim 1, in which said substrate is silicon and said liner material is selected from the group comprising $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$, and further comprising a step of:

epitaxially growing silicon on said interior walls and on said liner material after said step of etching said interior walls selective to said liner material.

4. (currently amended) A method according to claim ~~1~~ 2, further comprising a step of forming a vertical transistor having an active area overlapping said trench wall width and offset from said trench corners.

5. (original) A method according to claim 2, in which said first thickness is reduced to a second thickness after said step of etching said liner material selective to the substrate, said second thickness being such that remaining liner material protects {100} surfaces of said interior walls during said step of etching said interior walls selective to said liner material.

6. (original) A method according to claim 5, in which said step of etching said interior walls selective to said liner material is performed with an etchant including a compound from the group consisting of ammonia, tetramethyl ammonium hydroxide and a mixture of nitric and hydrofluoric acid.

7. (original) A method according to claim 4, in which said first thickness is reduced to a second thickness after said step of etching said liner material selective to the substrate, said second thickness being such that remaining liner material protects {100} surfaces of said interior walls during said step of etching said interior walls selective to said liner material.

8. (original) A method according to claim 7, in which said step of etching said interior walls selective to said liner material is performed with an etchant including a compound from the group consisting of ammonia, tetramethyl ammonium hydroxide and a mixture of nitric and hydrofluoric acid.

9. (original) A method according to claim 3, in which said first thickness is reduced to a second thickness after said step of etching said liner material selective to the substrate, said second thickness being such that remaining liner material protects {100} surfaces of said interior walls during said step of etching said interior walls selective to liner material.

10. (original) A method according to claim 9, in which said first thickness is reduced to a second thickness after said step of etching said liner material selective to the substrate, said second thickness being such that remaining liner material protects {100} surfaces of said interior walls during said step of etching said interior walls selective to said liner material.

11. (original) A method according to claim 2, in which said step of depositing a liner material is performed with UHVCVD.

12 - 20 (canceled)